1. A semiconductor structure comprising:

a semiconductor substrate; and

a dielectric layer located on said semiconductor substrate, such that an interface region is formed between semiconductor substrate and said dielectric layer;

a channel located proximate to said interface region, which channel is capable of carrying a current that varies from a first current value associated with a conducting condition, to a second current value associated with a non-conducting condition, said second current value being substantially less than said first current value;

a plurality of carrier trapping sites within said interface region, said carrier trapping sites being configured for trapping carriers that are electrically biased by an electrical control field to move from said channel into said interface region;

wherein said trapping sites have a concentration and arrangement so that said current in said channel can be varied between said first current value and said second current value by the action of said trapping sites adjusting said current in accordance with a value of said electrical control field.

2. The semiconductor structure of claim 1, wherein a trap energy level for said trapping sites is higher than a conduction band edge of said channel.

3. The semiconductor structure of claim 1, wherein said trap energy level is set so that said trapping sites trap primarily hot carriers flowing in said channel.

4. The semiconductor structure of claim 3, wherein said trap energy level is set to approximately .5 eV higher than said conduction band edge.

5. The semiconductor structure of claim 1, wherein said semiconductor structure is incorporated as part of an insulated gate field effect transistor.

6. The semiconductor structure of claim 1, wherein said carriers tunnel from said channel to said trapping sites.

7. The semiconductor structure of claim 6, wherein said carriers are not energized to tunnel from said channel to a conduction band of said interface region.

8. A negative differential resistance field effect transistor (NDR-FET) located within a substrate and having a control gate, a source region, a drain region and further comprising:

a channel located in a surface region of the substrate for carrying a source – drain current, said channel being configured so that carriers for said source-drain current in said channel can be subjected to an electrical field resulting from a bias voltage applied to the source and drain regions, and a control voltage applied to the control gate;

a gate insulation layer situated between said channel and the control gate;

an interface region located at a boundary of said gate insulation layer and said channel, and including a number of trapping sites adapted for temporarily storing carriers that acquire an amount of kinetic energy substantially equal to a trap energy level of said trapping sites, said trap energy level being greater than a conduction band energy level for said carriers;

wherein in a first operating region for the semiconductor device said source-drain current has a value that increases as said electrical field increases; and

further wherein in a second operating region for the semiconductor device said source-drain current has a value that decreases as said electrical field increases.

9. The device of claim 8, wherein said NDR FET shares one or more common structures with a conventional insulated gate field effect transistor (IGFET).

10. The device of claim 8, wherein said trapping sites include water based traps.

11. The device of claim 8, wherein said NDR FET uses an n-type channel implanted with a p-type dopant so that a relatively large electric bias field can be set up to facilitate moving said carriers from said channel to said trapping sites.

12. A semiconductor device located within a silicon on insulator (SO(I) substrate and having a control gate, a source region, a drain region and further comprising:

a channel located in a surface of the SOI substrate for carrying a source – drain current, said channel being configured so that carriers for said source-drain current in said channel can be subjected to an electrical field resulting from a bias voltage applied to the source and drain regions, and a control voltage applied to the control gate;

a trapping layer located close to said channel for temporarily storing carriers that acquire sufficient energy from said electrical field so that they can overcome a trapping energy level of carrier traps located in said trapping layer;

wherein in a first operating region for the semiconductor device said source-drain current has a value that increases as said electrical field increases; and

further wherein in a second operating region for the semiconductor device said source-drain current has a value that decreases as said electrical field increases.

13. The semiconductor device of claim 12, wherein said trapping layer is contained within an dielectric layer positioned between said channel and the control gate.

14. The semiconductor device of claim 12, wherein said trapping layer is contained within an interface region between said channel and a gate insulation layer for said semiconductor device.

15. The semiconductor device of claim 12, wherein said semiconductor device shares one or more common structures with a conventional insulated gate field effect transistor (IGFET).

16. In a memory cell including at least one first dopant type channel insulated gate field effect transistor (IGFET), the first-channel type IGFET having an IGFET gate terminal, a first IGFET source/drain terminal connected to a first potential, and a second IGFET source/drain terminal coupled to a storage node, the improvement comprising:

a negative differential resistance field-effect transistor (NDR-FET) element that also has a first dopant-type channel, said NDR FET element including a first NDR FET source/drain terminal connected to a second potential, a second NDR source/drain terminal connected to the storage node, and a third NDR gate terminal connected to a bias voltage;

wherein the NDR FET element operates as a pull-down device for the memory cell, so that the memory cell is formed entirely of active devices having a common channel dopant type.

17. The memory cell of claim 16, wherein said NDR FET element and the IGFET share at least a common substrate and a common gate insulation layer.

18. The memory cell of claim 16, wherein said third NDR gate terminal and said IGFET gate terminal are formed from the same conductive layer.

19. The memory cell of claim 16, wherein said storage node is a source/drain region shared by said NDR FET and the IGFET.

20. The memory cell of claim 16, wherein said first type dopant is n-type so that said NDR FET and the IGFET are n-channel devices.